1. Updating tanji3 documentation according to RTL, responsible for section2.1 to section2.3(KCE, LB, WB, Pooling Unit).

Reading RTL of data path to understand how the data is processed in different working modes.

Section I. Local Buffer (LB)

Understand how to assign values to control signals under different operating modes.

***GB2LB***

|  |  |  |
| --- | --- | --- |
| **signal** | **bit** | **value** |
| lb\_addr | 11 | bif\_lb\_gb2lb\_addr |
| lb\_wen | 16 | stgr\_enable\_row |
| lb\_wdata | 16 | bif\_lb\_gb2lb\_wdata |

***Convolution***

|  |  |  |
| --- | --- | --- |
| **signals** | **bit** | **value** |
| lb\_addr | 11 | int\_vert \* 36 + int\_hori |
| lb\_ren | 16 | stgr\_enable\_row |
| lb\_pad\_enable | 1 | bif\_lb\_conv\_pad\_enable |
| lb\_pad\_num | 1 | bif\_lb\_conv\_pad\_num |

***Full Connection***

|  |  |  |
| --- | --- | --- |
| **signals** | **bit** | **value** |
| lb\_addr | 11 | bif\_lb\_fc\_addr |
| lb\_ren | 16 | stgr\_enable\_row |

***Reshape***

|  |  |  |
| --- | --- | --- |
| **signals** | **bit** | **value** |
| lb\_addr | 11 | bif\_lb\_reshape\_addr |
| lb\_ren | 16 | stgr\_enable\_row |

Section II. Pooling unit

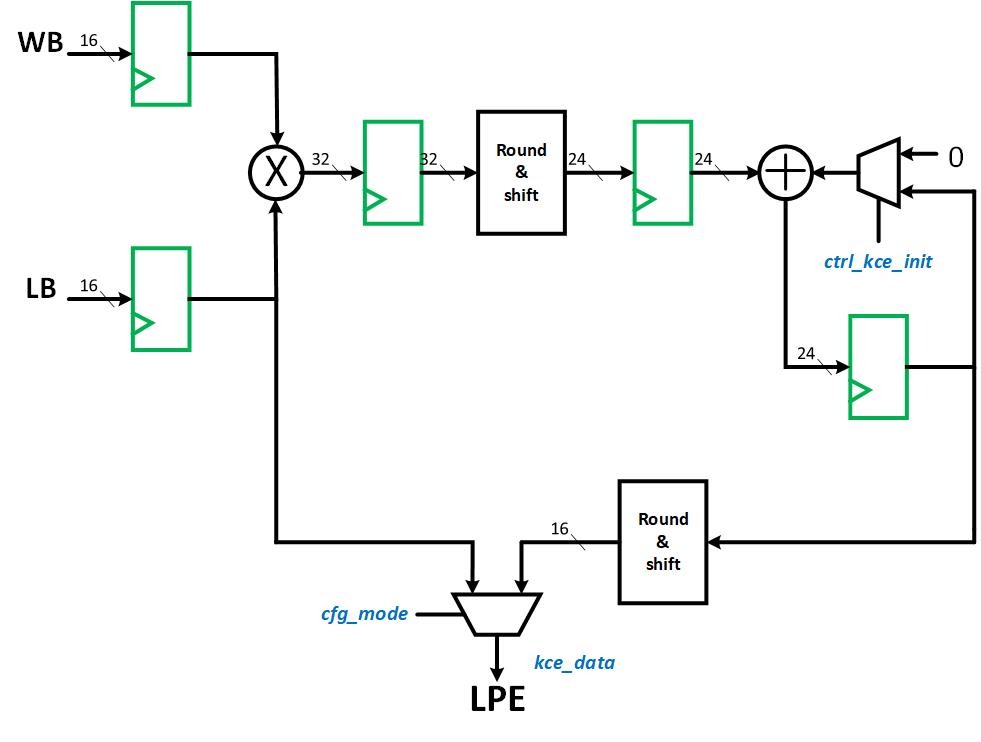


Compare input element to the data in its register, and store the larger or smaller according pooling mode. Each PU has one comparator inside. support *initial, stall*.

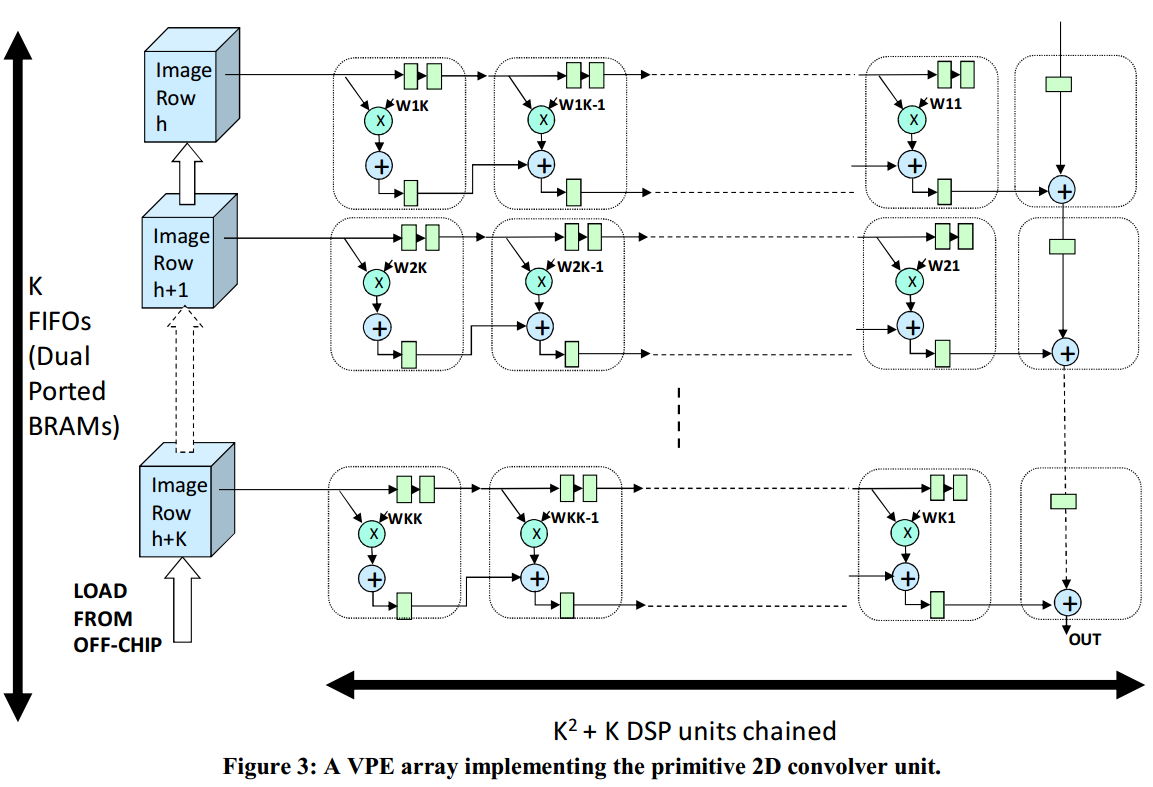
***initial:*** at the beginning of a pooling window, assign value to its register.

***stall:*** all registers hold the current data.

Section III. Kernel Computing Element (KCE)



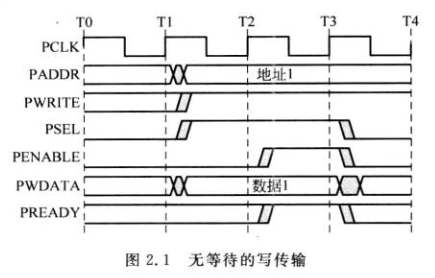
1. Read paper about Weight Stationary.



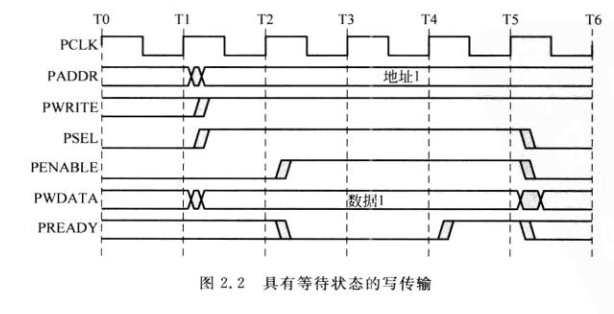
Each VPE consists of a multiply-accumulator (MAC), a programmable register holding a constant weight, and programmable input and output units. A VPE array implementing the primitive 2D convolver unit of k\*k.

1. Reading the documents for the AMBA and AXI bus to learn about their communication protocols, including AMBA APB, AMBA AHB and AXI4:

AMBA APB：



1. T1 period: Write transfers setup period. write address(PADDR), write data(PWDATA), write enable(PWRITE) and write select(PSEL) signals are registered on the rising edge.
2. T2 period: enable(PENABLE) and ready(PREADY) signals are registered on the rising edge: PENABLE represents the beginning of transfer access period. PREADY represents transfer can be completed in the next cycle. By control PREADY signal can extend tranfer.



|  |  |  |
| --- | --- | --- |
| signal | source | attribute |
| PCLK |  |  |
| PADDR | bus | address |
| PWDATA | bus | write data |
| PWRITE | bus | write enable 1: write  0: read |
| PSEL | bus | select slave device |
| PENABLE | slave | transfer enable signal |
| PRDATA | slave | read data |
| PREADY | slave | ready signal  1: transfers can be completed in the next period  0: wait until ready=1 |